CLAIMS

1. A method comprising:

defining a memory cell structure on a substrate;

depositing a layer of phosphorous doped oxide over the substrate;

selectively removing horizontal surfaces of the layer of phosphorous doped oxide while leaving vertical surfaces of the phosphorous doped oxide, wherein the horizontal surfaces are substantially planar to a surface of the substrate and the vertical surfaces are substantially perpendicular to the surface of the substrate.

2. The method of claim 1, wherein defining a memory cell utilizes photolithography and plasma etching.

3. The method of claim 1 further comprising selecting a thickness and phosphorus concentration of the phosphorous doped oxide to meet desirable performance parameters.

4. The method of claim 1 further comprising selecting a thickness and phosphorus concentration of the phosphorous doped oxed to result in a desired profile.

5. The method of claim 1, wherein selectively removing horizontal surfaces utilizes a directional plasma etch.

6. The method of claim 1, wherein the vertical surfaces comprise sidewalls along trench isolation area interfaces found along a self aligned source.

7. The method of claim 1, wherein the vertical surfaces comprise sidewalls of the memory cell.

8. A method comprising:

forming a self aligned source region and a drain region over a substrate;

selecting a thickness and phosphorous concentration for a phosphorous doped oxide layer;

depositing the phosphorous doped oxide layer over the substrate by means of chemical vapor deposition;

selectively removing horizontal surfaces of the phosphorous doped oxide layer while leaving vertical surfaces of the phosphorous doped oxide layer, wherein the horizontal surfaces are substantially planar to a substrate surface, the vertical surfaces are substantially perpendicular to the substrate surface and the vertical surfaces comprise sidewalls of the flash memory cell.

9. The method of claim 8, wherein the thickness and phosphorous concentration correspond to desired program rate, erase rate and data retention parameters.

10. The method of claim 8, wherein the thickness is in the range of 25Å to 500Å and the phosphorous concentration is in the range of 1% to 6%.

~~11. The method of claim 8, further comprising:~~

~~performing standard re-oxidation on the substrate.~~

~~12. A method for fabricating a flash memory cell comprising:~~

~~forming a self aligned source region in a substrate;~~

~~forming a drain region in the substrate;~~

~~depositing a layer of phosphorous doped oxide over the substrate;~~

~~selectively removing portions of the phosphorous doped oxide layer, leaving remaining portions of the phosphorous doped oxide layer; and~~

~~performing standard re-oxidation on the substrate.~~

~~13. A method for fabricating a flash memory cell comprising:~~

~~doping a drain region in a substrate with a first dopant;~~

~~doping a source region in the substrate with a second dopant;~~

~~depositing a layer of phosphorous doped oxide over the substrate according to a desired thickness and a desired phosphorus concentration;~~

~~selectively removing horizontal portions of the phosphorous doped oxide layer while leaving steep portions along steep exposed side walls; and~~

~~performing standard re-oxidation on the substrate.~~

14. The method of claim 13, wherein the steep exposed side-walls are sidewalls of shallow trench isolation (STI) trench and active areas interfaces along the source and a sidewall of the flash cell.

15. The method of claim 13, wherein the first dopant comprises boron-11 and the second dopant comprises phosphor-31 and arsenic-75.

16. A method of fabricating flash memory comprising:

defining a dimension of a flash cell on a substrate utilizing photolithography and plasma etching;

fabricating a drain region on the substrate;

fabricating a self aligned source region on the substrate;

depositing a thin layer of phosphorous doped oxide over the substrate having a thickness and phosphorous concentration;

performing a directional plasma etch to remove the doped oxide everywhere except along steep exposed side walls; and

performing a standard source drain re-oxidation process on the substrate.

17. The method of claim 16, wherein fabricating a self aligned source region comprises:

blocking a drain side of the flash cell;

performing an oxide dry etch in order to remove isolation oxide along the self-aligned source region;

implanting phosphor-31 to dope the self aligned source region;

implanting arsenic-75 to dope the self aligned source region; and

removing blocking from the drain side of the flash cell.

18. The method of claim 16, wherein fabricating a drain region comprises:

blocking a source side of the flash cell;

implanting boron-11; and

removing blocking from the source side.

19. A method of fabricating flash memory comprising:

defining a dimension of a flash cell on a substrate utilizing photolithography and plasma etching;

fabricating a drain in a drain region of the substrate by:

blocking a source region of the flash cell;

implanting boron-11; and

removing blocking from the source region;

fabricating a self aligned source in the source region of the substrate by:

blocking the drain region of the flash cell;

performing an oxide dry etch in order to remove isolation oxide along the self aligned source region;

implanting phosphor 31 to dope the self aligned source;

implanting arsenic 75 to dope the self aligned source; and

removing blocking from the drain region of the flash cell;

depositing a thin layer of phosphorous doped oxide, having a thickness and phosphorous concentration, over the substrate;

performing a directional plasma etch to remove the chemical vapor deposition oxide everywhere except along steep exposed side walls; and

performing a standard source drain re-oxidation process on the substrate.

20. The method of claim 19, further comprising selecting an erase rate by determining the thickness and phosphorous concentration of the phosphorous doped oxide.

21. The method of claim 19, further comprising selecting a self aligned source resistance according to the thickness and phosphorous concentration of the phosphorous doped oxide.

22. A method for fabricating memory cells;

providing a substrate;

forming a tunnel oxide layer over at least a portion of the substrate;

forming a first polysilicon layer over at least a portion of the substrate;

patterning the first polysilicon layer;

forming a dielectric layer over at least a portion of the substrate;

forming a second polysilicon layer over at least a portion of the substrate;

patterning the second polysilicon layer;

patterning one or more of the formed layers for a drain;

implanting the drain with a first dopant;

patterning one or more of the formed layers for a source;

implanting the source with a second dopant;

implanting the source with a third dopant;

depositing a phosphorous doped oxide layer having a thickness and a concentration over the substrate;

selectively removing portions of the phosphorous doped oxide layer leaving substantially vertical portions of the phosphorous doped oxide layer; and

performing a source/drain reoxidation.

23. The method of claim 22, wherein selectively removing portions of the phosphorous doped oxide layer utilizes an anisotropic etch.

24. The method of claim 22, wherein the substantially vertical portions are sidewalls of the memory cells.

~~25. The method of claim 22, wherein the memory cells utilize shallow trench isolation.~~

~~26. The method of claim 22, wherein the first polysilicon layer is a floating gate.~~

~~27. The method of claim 22, wherein the dielectric layer is an oxide-nitride-oxide.~~

~~28. The method of claim 22, wherein the second polysilicon layer is a wordline.~~

~~29. The method of claim 22, wherein the elements are performed in order.~~

~~30. The method of claim 22, wherein the first dopant is boron, the second dopant is phosphor and the third dopant is arsenic.~~

~~31. A method for fabricating memory cells;~~

~~providing a substrate;~~

~~forming a tunnel oxide layer over at least a portion of the substrate;~~

~~forming a first polysilicon layer over at least a portion of the tunnel oxide layer;~~

~~patterning the first polysilicon layer;~~

~~forming a dielectric layer over at least a portion of the first polysilicon layer;~~

~~forming a second polysilicon layer over at least a portion of the dielectric layer;~~

~~patterning the second polysilicon layer;~~

~~patterning one or more of the formed layers for a drain;~~

~~implanting the drain with boron;~~

~~patterning one or more of the formed layers for a source;~~

~~implanting the source with phosphor;~~

~~implanting the source with arsenic;~~

~~depositing a phosphorous doped oxide layer having a thickness and a concentration over the substrate;~~

~~selectively removing portions of the phosphorous doped oxide layer leaving substantially vertical portions of the phosphorous doped oxide layer;~~

~~performing a source/drain reoxidation;~~

~~implanting the source and the drain with arsenic; and~~

~~performing a source/drain anneal.~~

~~32.~~1. A semiconductor device comprising:

a substrate;

a drain formed in the substrate;

a ~~self aligned~~self-aligned source formed in the substrate;

a first oxide layer deposited over the substrate stretching from the drain to the ~~self aligned~~self-aligned source;

a first polysilicon deposited over the first oxide layer;

a second oxide layer deposited over the first polysilicon layer;

a second polysilicon layer deposited over the second oxide layer; and

a ~~phosphorous doped~~phosphorous-doped oxide along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer.

~~33.~~2. The semiconductor device of claim ~~32,~~1, wherein the first oxide layer is a tunnel oxide layer.

34. The semiconductor device of claim ~~32,~~1, wherein the second oxide layer is an oxide nitride oxide layer.

~~35.~~4. The semiconductor device of claim ~~32,~~1, wherein the first polysilicon layer is a floating gate.

~~36.~~5. The semiconductor device of claim ~~32,~~1, wherein the second polysilicon layer is a wordline.

~~37.~~6. A semiconductor device after re-oxidation comprising:

a substrate;

a drain formed in the substrate;

a ~~self aligned~~self-aligned source formed in the substrate;

a first oxide layer deposited over the substrate stretching from the drain to the ~~self aligned~~self-aligned source;

a first polysilicon layer deposited over the first oxide layer;

a second oxide layer deposited over the first polysilicon layer;

a second polysilicon layer deposited over the second oxide layer;

a phosphorous doped oxide layer along substantially ~~veritcal~~vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer; and

a re-oxidation oxide profile formed over surfaces of the semiconductor device having a height and width.

~~38.~~7. The device of claim ~~37,~~6, wherein the height is a vertical distance from the source to a bottom edge of the first polysilicon layer and the width is a horizontal distance from a side edge of the first polysilicon layer to a vertical edge of the tunnel oxide layer.

~~39.~~8. The device of claim ~~37,~~6, wherein the height and width are determined by characteristics of the phosphorous doped oxide.

~~40.~~9. A self aligned source of a flash memory device on a substrate, the self aligned source comprising:

one or more horizontal surfaces planar to the substrate having a desired doping concentration;

one or more vertical surfaces perpendicular and coupled to the one or more horizontal surfaces, the one or more vertical surfaces having a lower than desired doping concentration; and

one or more vertical ~~phosphorous doped~~phosphorous-doped oxide layers formed over the one or more vertical surfaces, the one or more vertical ~~phosphorous doped~~phosphorous-doped oxide layers having an additional doping concentration.

~~41.~~10. The self aligned source of claim ~~40,~~9, wherein the additional doping concentration and the less than desired doping concentration produce an effective doping concentration.

~~42.~~11. The self aligned source of claim ~~41,~~10, wherein the effective doping concentration is substantially equal to the desired doping concentration.

~~43.~~12. The self aligned source of claim ~~40,~~9, wherein the additional doping concentration, the less than desired doping concentration and the desired doping concentration are selected to provide a desired resistance.

~~44.~~13. A computer system comprising:

at least one processor;

a system bus;

a flash memory device coupled to the system bus, the memory device including one or more flash memory cells comprising:

a substrate;

a drain formed in the substrate;

a ~~self-aligned~~self-aligned source formed in the substrate;

a first oxide layer deposited over the substrate stretching from the drain to the ~~self aligned~~self-aligned source;

a first polysilicon deposited over the first oxide layer;

a second oxide layer deposited over the first polysilicon layer;

a second polysilicon layer deposited over the second oxide layer;

a phosphorous doped oxide along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer; and

a re-oxidation oxide profile formed over surfaces of the semiconductor device having a height and width.